

## CLAIMS

What is claimed is:

1. A transceiver circuit capable of transferring data at one or more transfer rates, the transceiver circuit comprising:
  3. one or more state machines having one or more tone phases in which determination of the maximum transfer rate for one or more channels and one or more connections with one or more remote devices is carried out through exchange of one or more tone signals with at least one of the remote device or devices, and one or more data transfer phases in which data transfer is carried out at one or more frequencies higher than that of at least one of the tone signal or signals;
  9. one or more error detection circuits detecting one or more errors in one or more receive signals; and
  11. one or more data transfer phase transition suppressor circuits;  
12. wherein, in the event that at least one of the error detection circuit or circuits detects at least one of the error or errors within at least one of the receive signal or signals during at least one of the data transfer phase or phases, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the data transfer phase transition suppressor circuit or circuits carries out control so as to prevent transition back to at least one of the data transfer phase or phases.
1. 2. A transceiver circuit according to claim 1 further comprising:
  2. one or more timers; and
  3. one or more error counters;  
4. wherein, only in the event that one or more numbers of errors occurring within one or more fixed times as detected by at least one of the error detection circuit or circuits, at least one of the timer or timers, and at least one of the error counter or counters during at least one of the data transfer phase or phases is greater than at least one preestablished value, one or more transitions is made from at least one of the data transfer phase or phases to at least one of the tone phase or phases, and after at least one of such transition or transitions has occurred, at least one of the data transfer phase transition suppressor

11 circuit or circuits carries out control so as to prevent transition back to at least one of the  
12 data transfer phase or phases.

1 3. A transceiver circuit according to claim 1 further comprising:

2 one or more transfer rate comparison circuits comparing the minimum transfer rate of  
3 which the transceiver circuit is capable and one or more transfer rates employed during at  
4 least one of the data transfer phase or phases;

5 wherein, only in the event that at least one of the error detection circuit or circuits  
6 detects at least one of the error or errors and at least one of the transition or transitions is  
7 made from at least one of the data transfer phase or phases to at least one of the tone  
8 phase or phases when at least one result of at least one comparison made by at least one  
9 of the transfer rate comparison circuit or circuits is that at least one of the transfer rate or  
10 rates employed during at least one of the data transfer phase or phases is identical to the  
11 minimum transfer rate or rates of which the transceiver circuit is capable, at least one of  
12 the data transfer phase transition suppressor circuit or circuits carries out control so as to  
13 prevent transition back to at least one of the data transfer phase or phases.

1 4. A transceiver circuit capable of transferring data at one or more transfer rates, the  
2 transceiver circuit comprising:

3 one or more state machines having one or more tone phases in which one or more  
4 connections with one or more remote devices are established through exchange of one or  
5 more tone signals with at least one of the remote device or devices, one or more speed  
6 negotiation phases in which determination of the maximum transfer rate permitted by  
7 one or more channels is carried out through mutual notification of one or more transfer  
8 rates of which the local device is capable, this notification being actually carried out at at  
9 least one of such transfer rate or rates, and one or more data transfer phases in which data  
10 transfer is carried out at at least one of the transfer rate or rates determined at at least one  
11 of the speed negotiation phase or phases;

12 one or more error detection circuits detecting one or more errors in one or more  
13 receive signals; and

14 one or more speed negotiation phase transition suppressor circuits;

15 wherein, in the event that at least one of the error detection circuit or circuits detects  
16 at least one of the error or errors within at least one of the receive signal or signals during

17 at least one of the data transfer phase or phases, one or more transitions is made from at  
18 least one of the data transfer phase or phases to at least one of the tone phase or phases,  
19 and after at least one of such transition or transitions has occurred, at least one of the  
20 speed negotiation phase transition suppressor circuit or circuits carries out control so as  
21 to prevent transition to at least one of the speed negotiation phase or phases.

1 5. A transceiver circuit capable of transferring data at one or more transfer rates, the  
2 transceiver circuit comprising:

3 one or more state machines having one or more tone phases in which one or more  
4 connections with one or more remote devices are established through exchange of one or  
5 more tone signals with at least one of the remote device or devices, one or more speed  
6 negotiation phases in which determination of one or more maximum transfer rates  
7 permitted by one or more channels is carried out through mutual notification of one or  
8 more transfer rates of which the local device is capable, this notification being actually  
9 carried out at at least one of such transfer rate or rates, and one or more data transfer  
10 phases in which data transfer is carried out at at least one of the transfer rate or rates  
11 determined at at least one of the speed negotiation phase or phases;

12 one or more error detection circuits detecting one or more errors in one or more  
13 receive signals; and

14 one or more speed negotiation phase transition suppressor circuits;

15 wherein, in the event that at least one of the error detection circuit or circuits detects  
16 at least one of the error or errors within at least one of the receive signal or signals during  
17 at least one of the speed negotiation phase or phases, one or more transitions is made  
18 from at least one of the data transfer phase or phases to at least one of the tone phase or  
19 phases, and after at least one of such transition or transitions has occurred, at least one of  
20 the speed negotiation phase transition suppressor circuit or circuits carries out control so  
21 as to prevent transition to at least one of the speed negotiation phase or phases.

1 6. A transceiver circuit according to claim 4 or 5 further comprising:

2 one or more timers; and

3 one or more error counters;

4 wherein, only in the event that one or more numbers of errors occurring within one or  
5 more fixed times as detected by at least one of the error detection circuit or circuits, at

6       least one of the timer or timers, and at least one of the error counter or counters is greater  
7       than at least one preestablished value, one or more transitions is made from at least one  
8       of the data transfer phase or phases to at least one of the tone phase or phases, and after  
9       at least one of such transition or transitions has occurred, at least one of the state machine  
10      phase transition suppressor circuit or circuits carries out control so as to prevent  
11      transition to at least one of the speed negotiation phase or phases.

1       7. A transceiver circuit according to claim 4 or 5 further comprising:  
2           one or more transfer rate comparison circuits comparing minimum transfer rate of  
3           which the transceiver circuit is capable and one or more transfer rates employed during at  
4           least one of the data transfer phase or phases;  
5           wherein, only in the event that at least one of the error detection circuit or circuits  
6           detects at least one of the error or errors and at least one of the transition or transitions is  
7           made from at least one of the data transfer phase or phases to at least one of the tone  
8           phase or phases when at least one result of at least one comparison made by at least one  
9           of the transfer rate comparison circuit or circuits is that at least one of the transfer rate or  
10          rates employed during at least one of the data transfer phase or phases is identical to at  
11          least one of the minimum transfer rate or rates of which the transceiver circuit is capable,  
12          at least one of the speed negotiation phase transition suppressor circuit or circuits carries  
13          out control so as to prevent transition to at least one of the speed negotiation phase or  
14          phases.

1       8. A transceiver circuit according to claim 4 or 5 further comprising:  
2           one or more counters; and  
3           one or more timers;  
4           wherein the transceiver circuit is OP iLINK-compliant;  
5           wherein at least one of the counter or counters counts one or more numbers of  
6           transitions from at least one of the tone phase or phases to at least one of the speed  
7           negotiation phase or phases; and  
8           wherein, in the event that at least one of the number or numbers of transitions as  
9           counted by at least one of the counter or counters reaches at least one preestablished  
10          value within at least one fixed time, it being determined that channel quality is poor, at  
11          least one of the speed negotiation phase transition suppressor circuit or circuits carries

12       out control so as to prevent transition to at least one of the speed negotiation phase or  
13       phases.

1       9.      A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:

2             one or more tone signal transmit select circuits are employed as at least one of the  
3             data transfer phase transition suppressor circuit or circuits or speed negotiation phase  
4             transition suppressor circuit or circuits; and

5             in the event that at least one of the error detection circuit or circuits determines that  
6             channel quality is poor and one or more transitions is made from at least one of the data  
7             transfer phase or phases to at least one of the speed negotiation phase or phases, at least  
8             one of the tone signal transmit select circuit or circuits carries out control so as to prevent  
9             transmission of one or more tone signals.

1       10.     A transceiver circuit according to claim 9 further comprising:

2             one or more receive signal detection circuits; and

3             one or more timers;

4             wherein, in the event that at least one of the receive signal detection circuit or circuits  
5             and at least one of the timer or timers establish during at least one of the tone phase or  
6             phases that at least one receive signal, being absent for not less than at least one fixed  
7             time, has been completely disconnected, at least one of the tone signal transmit select  
8             circuit or circuits reinitiates transmission of one or more tone signals.

1       11.     A transceiver circuit according to claim 9 further comprising:

2             one or more cable connect detection circuits;

3             wherein, in the event that at least one of the cable connect detection circuit or circuits  
4             establishes during at least one of the tone phase or phases that one or more cables has  
5             been disconnected, at least one of the tone signal transmit select circuit or circuits  
6             reinitiates transmission of one or more tone signals after at least one of the cable or  
7             cables has been reconnected.

1       12.     A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:

2             one or more transmitter power supply control circuits are employed as at least one of  
3             the data transfer phase transition suppressor circuit or circuits or speed negotiation phase  
4             transition suppressor circuit or circuits; and

5             in the event that at least one of the error detection circuit or circuits determines that

6 channel quality is poor, one or more transitions is made to at least one of the tone phase  
7 or phases, and after at least one of such transition or transitions has occurred, at least one  
8 of the transmitter power supply control circuit or circuits causes at least one power  
9 supply of at least one transmitter to be turned OFF.

13. A transceiver circuit according to claim 12 further comprising:

one or more receive signal detection circuits; and

one or more timers;

wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time, has been completely disconnected, at least one of the transmitter power supply control circuit or circuits causes at least one power supply of at least one transmitter to be turned ON.

14. A transceiver circuit according to claim 12 further comprising:

one or more cable connect detection circuits;

wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the transmitter power supply control circuit or circuits causes at least one power supply of at least one transmitter to be turned ON after at least one of the cable or cables has been reconnected.

15. A transceiver circuit according to claim 6, 7, or 8 wherein:

the transceiver circuit is OP iLINK-compliant;

one or more TPBIAS mask circuits provided at one or more PORT locations is or are employed as at least one of the speed negotiation phase transition suppressor circuit or circuits; and

in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, one or more transitions is made to at least one of the tone phase or phases, and thereafter at least one of the TPBIAS mask circuit or circuits masks one or more TPBIAS signals from at least one PHY carries out control so as to prevent transmission of one or more long tones and/or one or more continuous signals even if at least one TPBIAS is active.

1       16. A transceiver circuit according to claim 15 further comprising:

2              one or more receive signal detection circuits; and

3              one or more timers;

4              wherein, in the event that at least one of the receive signal detection circuit or circuits

5              and at least one of the timer or timers establish during at least one of the tone phase or

6              phases that at least one receive signal, being absent for not less than at least one fixed

7              time following transmission of one or more tone signals by one or more local transmit

8              circuits, has been completely disconnected, at least one of the mask or masks applied to

9              at least one of the TPBIAS signal or signals by at least one of the TPBIAS mask circuit

10             or circuits is removed, causing one or more long tone signals and/or one or more

11             continuous signals to be transmitted when at least one TPBIAS is active.

1       17. A transceiver circuit according to claim 15 further comprising:

2              one or more cable connect detection circuits;

3              wherein, in the event that at least one of the cable connect detection circuit or circuits

4              establishes during at least one of the tone phase or phases that one or more cables has

5              been disconnected, at least one of the mask or masks applied to at least one of the

6              TPBIAS signal or signals by at least one of the TPBIAS mask circuit or circuits is

7              removed after at least one of the cable or cables has been reconnected, causing one or

8              more long tone signals and/or one or more continuous signals to be transmitted when at

9              least one TPBIAS is active.

1       18. A transceiver circuit according to claim 6, 7, or 8 wherein:

2              the transceiver circuit is OP iLINK-compliant;

3              one or more TPBIAS suppressor circuits provided at one or more PHY locations is or

4              are employed as at least one of the speed negotiation phase transition suppressor circuit

5              or circuits; and

6              in the event that at least one of the error detection circuit or circuits determines that

7              channel quality is poor, one or more transitions is made to at least one of the tone phase

8              or phases, and thereafter, even if at least one TPBIAS is active within at least one of the

9              PHY location or locations, at least one of the TPBIAS suppressor circuit or circuits

10             carries out control so as to prevent at least one of the PORT location or locations from

11             being notified of the fact that the at least one TPBIAS is active.

1        19. A transceiver circuit according to claim 18 further comprising:  
2              one or more receive signal detection circuits; and  
3              one or more timers;  
4              wherein, in the event that at least one of the receive signal detection circuit or circuits  
5              and at least one of the timer or timers establish during at least one of the tone phase or  
6              phases that at least one receive signal, being absent for not less than at least one fixed  
7              time following transmission of one or more tone signals by one or more local transmit  
8              circuits, has been completely disconnected, at least one of the TPBIAS suppressor circuit  
9              or circuits causes at least one of the PORT location or locations to be notified of at least  
10             one value of at least one TPBIAS signal within at least one of the PHY location or  
11             locations.

1        20. A transceiver circuit according to claim 18 further comprising:  
2              one or more cable connect detection circuits;  
3              wherein, in the event that at least one of the cable connect detection circuit or circuits  
4              establishes during at least one of the tone phase or phases that one or more cables has  
5              been disconnected, at least one of the TPBIAS suppressor circuit or circuits, after at least  
6              one of the cable or cables has been reconnected, causes at least one of the PORT location  
7              or locations to be notified of at least one value of at least one TPBIAS signal within at  
8              least one of the PHY location or locations.

1        21. A transceiver circuit according to claim 6, 7, or 8 wherein:  
2              the transceiver circuit is OP iLINK-compliant;  
3              one or more BIAS\_DETECT suppressor circuits provided at one or more PORT  
4              locations is or are employed as at least one of the speed negotiation phase transition  
5              suppressor circuit or circuits; and  
6              in the event that at least one of the error detection circuit or circuits determines that  
7              channel quality is poor, one or more transitions is made to at least one of the tone phase  
8              or phases, and thereafter, even if one or more long tones and/or one or more continuous  
9              signals is or are received from one or more remote devices by at least one of the PORT  
10             location or locations and at least one BIAS\_DETECT is active, at least one of the  
11             BIAS\_DETECT suppressor circuit or circuits carries out control so as to prevent at least

12        one of one PHY location or locations from being notified of the fact that the at least one  
13        BIAS\_DETECT is active.

1        22. A transceiver circuit according to claim 21 further comprising:  
2              one or more receive signal detection circuits; and  
3              one or more timers;  
4              wherein, in the event that at least one of the receive signal detection circuit or circuits  
5              and at least one of the timer or timers establish during at least one of the tone phase or  
6              phases that at least one receive signal, being absent for not less than at least one fixed  
7              time following transmission of one or more tone signals by one or more local transmit  
8              circuits, has been completely disconnected, at least one of the BIAS\_DETECT  
9              suppressor circuit or circuits causes at least one of the PHY location or locations to be  
10             notified of at least one value of at least one BIAS\_DETECT signal within at least one of  
11             the PORT location or locations.

1        23. A transceiver circuit according to claim 21 further comprising:  
2              one or more cable connect detection circuits;  
3              wherein, in the event that at least one of the cable connect detection circuit or circuits  
4              establishes during at least one of the tone phase or phases that one or more cables has  
5              been disconnected, at least one of the BIAS\_DETECT suppressor circuit or circuits, after  
6              at least one of the cable or cables has been reconnected, causes at least one of the PHY  
7              location or locations to be notified of at least one value of at least one BIAS\_DETECT  
8              signal within at least one of the PORT location or locations.

1        24. A transceiver circuit according to claim 6, 7, or 8 wherein:  
2              the transceiver circuit is OP iLINK-compliant;  
3              one or more BIAS\_DETECT mask circuits provided at one or more PHY locations is  
4              or are employed as at least one of the speed negotiation phase transition suppressor  
5              circuit or circuits; and  
6              in the event that at least one of the error detection circuit or circuits determines that  
7              channel quality is poor, one or more transitions is made to at least one of the tone phase  
8              or phases, and thereafter, even if one or more BIAS\_DETECT signals is active, masking  
9              by at least one of the BIAS\_DETECT mask circuit or circuits of at least one  
10             BIAS\_DETECT signal from at least one of the PORT location or locations carries out

control so as to prevent at least one of the PHY location or locations from being notified of the fact that the at least one BIAS\_DETECT signal is active.

25. A transceiver circuit according to claim 24 further comprising:  
one or more receive signal detection circuits; and  
one or more timers;  
wherein, in the event that at least one of the receive signal detection circuit or circuits and at least one of the timer or timers establish during at least one of the tone phase or phases that at least one receive signal, being absent for not less than at least one fixed time following transmission of one or more tone signals by one or more local transmit circuits, has been completely disconnected, at least one of the mask or masks applied to at least one of the BIAS\_DETECT signal or signals by at least one of the BIAS\_DETECT mask circuit or circuits is removed, causing at least one of the PHY location or locations to be notified of the fact that at least one BIAS\_DETECT is active when the at least one BIAS\_DETECT is active.

26. A transceiver circuit according to claim 24 further comprising:  
one or more cable connect detection circuits;  
wherein, in the event that at least one of the cable connect detection circuit or circuits establishes during at least one of the tone phase or phases that one or more cables has been disconnected, at least one of the mask or masks applied to at least one of the BIAS\_DETECT signal or signals by at least one of the BIAS\_DETECT mask circuit or circuits is removed after at least one of the cable or cables has been reconnected, causing at least one of the PHY location or locations to be notified of the fact that the at least one BIAS\_DETECT is active when the at least one BIAS\_DETECT is active.

27. A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:  
the transceiver circuit is IEEE 1394-compliant;  
one or more suspend/disable control circuits provided at one or more PHY locations is or are employed as at least one of the speed negotiation phase transition suppressor circuit or circuits; and  
in the event that at least one of the error detection circuit or circuits determines that channel quality is poor, at least one of the suspend/disable control circuit or circuits, during at least one of the tone phase or phases, causes at least one PORT at which at least

9       one error is or was detected to enter at least one suspended state and/or at least one  
10      disabled state.

1       28. A transceiver circuit according to claim 27 further comprising:  
2           one or more receive signal detection circuits; and  
3           one or more timers;  
4           wherein, in the event that at least one of the receive signal detection circuit or circuits  
5           and at least one of the timer or timers establish during at least one of the tone phase or  
6           phases that at least one receive signal, being absent for not less than at least one fixed  
7           time following transmission of one or more tone signals by one or more local transmit  
8           circuits, has been completely disconnected, at least one of the suspend/disable control  
9           circuit or circuits causes termination of at least one suspended state and/or at least one  
10          disabled state.

1       29. A transceiver circuit according to claim 27 further comprising:  
2           one or more cable connect detection circuits;  
3           wherein, in the event that at least one of the cable connect detection circuit or circuits  
4           establishes during at least one of the tone phase or phases that one or more cables has  
5           been disconnected, at least one of the suspend/disable control circuit or circuits causes  
6           termination of at least one suspended state and/or at least one disabled state after at least  
7           one of the cable or cables has been reconnected.

1       30. A transceiver circuit according to claim 2, 3, 6, 7, or 8 wherein:  
2           one or more wait states is or are present between at least one of the data transfer phase  
3           or phases and at least one of the tone phase or phases; and  
4           in the event that at least one of the error detection circuit or circuits determines that  
5           channel quality is poor, one or more transitions is made from at least one of the data  
6           transfer phase or phases to at least one of the wait state or states, and only if it is  
7           established during at least one of the wait state or states that at least one remote device  
8           has been completely disconnected therefrom is at least one transition made to at least one  
9           of the tone phase or phases.

1       31. A transceiver circuit according to claim 30 further comprising:  
2           one or more receive signal detection circuits; and  
3           one or more timers;

4           wherein, in the event that at least one of the receive signal detection circuit or circuits  
5           and at least one of the timer or timers establish during at least one of the tone phase or  
6           phases that at least one receive signal, being absent for not less than at least one fixed  
7           time following transmission of one or more tone signals by one or more local transmit  
8           circuits, has been completely disconnected, at least one transition is made from at least  
9           one of the wait state or states back to at least one of the tone phase or phases.

1       32. A transceiver circuit according to claim 30 further comprising:  
2           one or more cable connect detection circuits;  
3           wherein, in the event that at least one of the cable connect detection circuit or circuits  
4           establishes during at least one of the tone phase or phases that one or more cables has  
5           been disconnected, at least one transition is made from at least one of the wait state or  
6           states back to at least one of the tone phase or phases after at least one of the cable or  
7           cables has been connected.

1       33. A transceiver circuit capable of transferring data at a plurality of transfer rates, the  
2           transceiver circuit comprising:  
3           one or more state machines having one or more tone phases in which one or more  
4           connections with one or more remote devices are established through exchange of one or  
5           more tone signals with at least one of the remote device or devices, one or more speed  
6           negotiation phases in which determination of the maximum transfer rate permitted by  
7           one or more channels is carried out through mutual notification of one or more transfer  
8           rates of which one or more local devices is capable, this notification being actually  
9           carried out at at least one of such transfer rate or rates, and one or more data transfer  
10          phases in which data transfer is carried out at at least one of the transfer rate or rates  
11          determined at at least one of the speed negotiation phase or phases;  
12          one or more error detection circuits detecting one or more errors in one or more  
13          receive signals; and  
14          one or more transfer rate comparison circuits comparing the minimum transfer rate of  
15          the transceiver circuit and one or more transfer rates employed during at least one of the  
16          data transfer phase or phases;  
17          wherein, in the event that at least one of the error detection circuit or circuits detects  
18          at least one of the error or errors within at least one of the receive signal or signals during

19 at least one of the data transfer phase or phases when at least one result of at least one  
20 comparison made by at least one of the transfer rate comparison circuit or circuits is that  
21 at least one of the transfer rate or rates employed during at least one of the data transfer  
22 phase or phases is greater than the minimum transfer rate or rates of the transceiver  
23 circuit, one or more transitions is made from at least one of the data transfer phase or  
24 phases to at least one of the tone phase or phases, and thereafter, the maximum transfer  
25 rate of the transceiver circuit during at least one of the speed negotiation phase or phases  
26 is set so as to be at least one rate that is lower than at least one transfer rate employed  
27 during at least one of the data transfer phase or phases.

1 34. A transceiver circuit according to claim 33 further comprising:

2 one or more receive signal detection circuits; and

3 one or more timers;

4 wherein, in the event that at least one of the receive signal detection circuit or circuits  
5 and at least one of the timer or timers establish during at least one of the tone phase or  
6 phases that at least one receive signal, being absent for not less than at least one fixed  
7 time following transmission of one or more tone signals by one or more local transmit  
8 circuits, has been completely disconnected, the maximum transfer rate of the transceiver  
9 circuit during at least one of the speed negotiation phase or phases is returned to its  
10 original maximum transfer rate.

1 35. A transceiver circuit according to claim 33 further comprising:

2 one or more cable connect detection circuits;

3 wherein, in the event that at least one of the cable connect detection circuit or circuits  
4 establishes during at least one of the tone phase or phases that one or more cables has  
5 been disconnected, the maximum transfer rate of the transceiver circuit during at least  
6 one of the speed negotiation phase or phases is returned to its original maximum transfer  
7 rate after at least one of the cable or cables has been reconnected.

1 36. A transceiver circuit according to claim 10 or 13 wherein the at least one fixed time is  
2 not less than 132 ms.

1 37. A transceiver circuit according to claim 16, 19, 22, 25, 28, 31, or 34 wherein the at  
2 least one fixed time is not less than 64 ms and not more than 132 ms.

1       38. A transceiving method substantially effects manifestation of one or more transceiver  
2       circuits according to any one of claims 1 through 37.

1       39. A transceiver apparatus comprising:  
2             one or more transceiver circuits substantially according to any one of claims 1 through  
3             37; and  
4             one or more external display apparatuses;  
5             wherein, in the event that at least one of the error detection circuit or circuits  
6       determines that channel quality is poor during at least one of the data transfer phase or  
7       phases or speed negotiation phase or phases, and at least one of the transceiver circuit or  
8       circuits is in one or more suppressed states selected from among the group consisting of  
9       suppression with respect to transition to at least one of the data transfer phase or phases,  
10      suppression with respect to transition to at least one of the speed negotiation phase or  
11      phases, and suppression with respect to maximum transfer rate during at least one of the  
12      speed negotiation phase or phases, one or more users are notified of such fact by means  
13      of at least one of the external display apparatus or apparatuses.